High-Resolution 32 Channel TDC
(< 10 ps RMS)
Implemented in FPGA

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Outline

1. Motivation
2. Method
3. Design
4. Results
5. Comparison with other TDCs
Motivation

FPGA-TDC:

- Fast development process
- Flexible (Clock frequency, resolution/channel Nr. trade-off)
- Adaptable (Special needs, e.g: extra large FIFOs for bursts)

Previous work in this field, e.g.:

- 1997: Kalisz, Altera Quick Logic, 200 ps resolution
- 2008: J.Wu, Altera-Cyclone-II, 10 ps RMS
- 2009: Favi, Virtex-5, ~ 17 ps resolution
The Method

The Nutt method:
- 1 Stage: Counter
- 2 Stage: Interpolator

Interpolation:
- Here: Tapped Delay Lines method

Idea:
- The asynchronous input signal (e.g. one rising edge) runs through a chain of delay elements
- The position of the 0/1 transition is stored in the FF array at the next rising edge of the system clock

\[
T_{DIFF} = T_A + (T_{SYS} - T_B) + (S_A - S_B) \cdot T_{SYS}
\]
Tapped Delay Lines in FPGA

**FPGA:**
- The "Carry-Chain" serves as a delay chain
- Carry-Chain multiplexers are the delay elements
- Delay (max.) = 45 ps (Virtex-4: CIN→COUT = 90 ps, speed grade 10)
- Real delays vary → cell-by-cell calibration necessary
- Problem: The “Ultra Wide Bins” (J.Wu)
Typical Problem:
- Large delay variance
- Some delays are "ultra" wide
  → Bad DNL and INL

Idea [J.Wu]: Wave Union
- Use multiple edges in one chain!
  → Reduces the ultra wide delays
  → Resolution improvement possible
Wave Union Method:
- Two or more transitions propagate.
- If one transition is in an ultra wide bin, then the other is in a normal bin.

Procedure:
- Store a pattern of edges
- Trigger them simultaneously
  → Control the runtime of signals
  (difficult but feasible)

Consequence:
Ultra wide bins become smaller.
Design (one TDC-channel, simplified)

Interpolator
Dual-Syncronizer

Trigger

FF_array
carry_chain

Decoder
FIFO
Control

... to FPGA_TOP ...

signal

sys_clk

sys_clk

sys_clk
Measurements

**Measured:**
1. Root Mean Square \( RMS = \sqrt{\frac{\sum_{i=1}^{N} (x_i - \bar{x})^2}{N}} \)
2. Temperature dependence
3. Dependence on the supply voltage variations
4. Crosstalk

**Measurement setup:**
- Delay between 2 rising edges on different channels
- \( \sim 250k \) measurements pro setup.
- Delays < 1 ns were adjusted via different cable lengths
- Delays > 1 ns were adjusted with the Tektronix Data Timing Generator (precision = 1 ps)
- Measurement value: Sum of positions + timestamp
- Calibration and analysis offline
**RMS**

- **3 measurement series**: the async. edges arrive...
  1. ... within one period of the system clock.
  2. ... with an offset of multiple sys_clk cycles.
  3. ... with offset > 1 µs.

- **Test reading**:

<table>
<thead>
<tr>
<th>wire length channel A</th>
<th>mean [ps]</th>
<th>RMS [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>~6 cm</td>
<td>1697</td>
<td>9</td>
</tr>
<tr>
<td>~7 cm</td>
<td>1740</td>
<td>9</td>
</tr>
<tr>
<td>~8 cm</td>
<td>1781</td>
<td>9</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DTG time diff. [ns]</th>
<th>mean [ps]</th>
<th>RMS [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>45798</td>
<td>9</td>
</tr>
<tr>
<td>44</td>
<td>47798</td>
<td>9</td>
</tr>
<tr>
<td>46</td>
<td>49798</td>
<td>9</td>
</tr>
<tr>
<td>1004</td>
<td>1005795</td>
<td>11</td>
</tr>
<tr>
<td>1006</td>
<td>1007797</td>
<td>11</td>
</tr>
<tr>
<td>1008</td>
<td>1009798</td>
<td>11</td>
</tr>
</tbody>
</table>
Temperature Variation

- **Temperature region**: 30 °C – 85 °C in 5°C steps.

- **Observations**:
  1. Deformation of the calibration LUTs.
  2. Measured distance in delay elements changes, but...
  3. ...no change of the calibrated value of the RMS, if calibration LUT is up-to-date. (acceptable region: ± 5°C)

- **Conclusion**: No significant effect!
Core Voltage Variation

- **Region**: 1.15 V – 1.25 V
- **Observations**:
  1. Deformation of the calibration LUTs
  2. 2 ps increase of the RMS value
  3. 40 ps shift of the mean in the whole region
- **Conclusion**:
  - The voltage has to be stabilized
  - Worst case ± 12 mV
    → ca. 7 ps
  - (Normal case: ± 2 mV)
No crosstalk under normal conditions

Prove of sensitivity with enforced crosstalk (flat band cable)
## Usage of Resources

<table>
<thead>
<tr>
<th>Resource</th>
<th>Used</th>
<th>Available</th>
<th>In %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slice-Register</td>
<td>22.096</td>
<td>36.864</td>
<td>59</td>
</tr>
<tr>
<td>LUTs</td>
<td>18.119</td>
<td>36.864</td>
<td>49</td>
</tr>
<tr>
<td>Block-RAM</td>
<td>37</td>
<td>96</td>
<td>38</td>
</tr>
</tbody>
</table>
Comparison with other TDCs

FPGA-TDC (GSI):
- 32 channel with 9 ps RMS for a time difference measurement (6 ps resolution per channel), dead time: 8 cycles @ 200 MHz unpipelined, 2 cycles pipelined (to be done)

FPGA-TDC (J.Wu):
- 18 channels with 25 ps RMS, dead time: 2 cycles @ 400 MHz
- 8 channels with 10 ps RMS, dead time: 18 cycles @ 400 MHz

HP-TDC (CERN):
- 32 channels with 30 ps resolution
- 8 channels with 17 ps resolution

TDC-GPX (Fa. ACAM):
- 8 channels with 27 ps resolution, 200 MHz max. Hit rate (40 MHz continuous)
- 2 channels with 10 ps resolution, dead time 18 cycles, 500 kHz continuous hit rate
Thanks for your attention!